Challenges and Opportunities with Gate-All-Around Transistors

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Abstract

Gate-all-around (GAA) transistors have emerged as a critical enabler for scaling semiconductor devices beyond the 5 nm technology node. By fully surrounding the channel with gate material, GAA architectures offer superior electrostatic control, reduced short-channel effects, and improved drive current compared to FinFETs—the previous industry standard. Despite their promise, the widespread adoption of GAA transistors faces significant challenges, including increased thermal confinement, complex fabrication requirements, and reliability concerns such as inner spacer degradation. Addressing these obstacles requires coordinated advancements in materials engineering, process integration, and device design. Ongoing research in both academic and industrial settings is rapidly advancing the GAA landscape, with innovations that aim to make these devices viable for next-generation logic technologies.

I. INTRODUCTION

Complementary metal-oxide-semiconductor (CMOS) technology has been the foundation of semiconductor devices for decades. As the demand for smaller, faster, and more energy-efficient electronics continues to grow, the need to scale CMOS technology has become increasingly critical to sustaining Moore's law. The push for improved device performance and reduced power consumption led to the development of Fin field-effect transistors (FinFETs), which introduced superior electrostatic control by wrapping the gate around three sides of the channel. FinFETs successfully enabled scaling down to the 5 nm node, but this architecture now faces physical and performance limitations at smaller dimensions.

In response, gate-all-around field-effect transistors (GAAFETs) have emerged as a promising successor, as seen in Fig. 1.

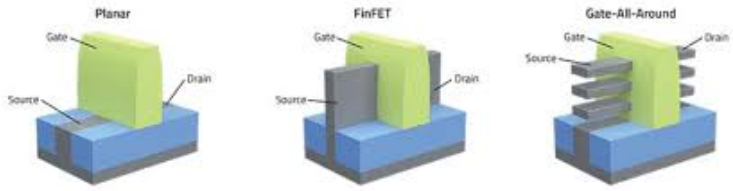

Figure 1: Illustration of a gate-all-around field-effect transistor (GAAFET) structure.

By surrounding the channel on all sides with gate material, GAAFETs offer improved electrostatic integrity, higher drive current, and enhanced scalability compared to FinFETs[3]. However, the transition to GAAFETs introduces new engineering challenges in device design, fabrication, and reliability. Critical issues include complex multi-layer nanosheet stacking, inner spacer integrity, and increased thermal confinement due to the device geometry.

Addressing these challenges is paramount to realizing the full potential of GAAFET technology in advanced logic nodes. This paper provides an overview of key obstacles to GAAFET adoption and highlights recent advances from both academic and industrial research aimed at enabling reliable, scalable implementation.

II. ENGINEERING CHALLENGES IN GAA DEVELOPMENT

With the experimental success and increasing momentum toward mainstream adoption of gate-all-around field-effect transistors (GAAFETs), engineers and researchers face a range of technical challenges. These challenges stem primarily from the unique vertically stacked nanosheet structure of GAAFETs and the aggressive push toward sub-5 nm technology nodes. While GAAFETs offer substantial advantages over FinFETs—including superior electrostatic control and improved scalability—successful integration into manufacturing requires overcoming critical barriers in fabrication precision, device reliability, and thermal management. This section outlines several of the key engineering challenges hindering the seamless adoption of GAAFETs.

A. Fabrication and Integration

GAAFETs are composed of vertically stacked nanosheet channels, fully surrounded by a gate material on all sides. Fabricating these three-dimensional, multilayer structures with tight control over sheet thickness, spacing, and release is inherently complex [3]. Variability in these parameters can result in inconsistent electrical characteristics and degraded device performance across a wafer or die.

One of the most demanding steps is the selective etching of sacrificial silicon–germanium (SiGe) layers to release the silicon nanosheets. This process requires extremely high selectivity and precision to avoid damage to the remaining channel or surrounding materials. Additionally, forming conformal gate stacks that wrap around each nanosheet necessitates the use of advanced deposition techniques, such as atomic layer deposition (ALD), to precisely control sidewall profiles and ensure gate uniformity. Despite sharing some process elements with FinFET fabrication, the integration of GAAFETs into existing CMOS workflows remains a challenge. Conventional workflows are not fully optimized for multilayer

nanosheet structures, and the additional complexity introduced by stacking demands tighter control over epitaxy, etching, and gate formation steps[5].

B. Inner Spacer Reliability

Unlike FinFETs, GAAFETs incorporate an inner spacer—an insulating region between the gate and the source/drain epitaxy. This component plays a vital role in suppressing parasitic capacitance and enabling self-aligned junction formation. However, it also introduces new reliability risks. IBM and Micromachines found that under prolonged electrical and thermal stress, this region is prone to breakdown compromising electrical isolation and mechanical stability over hours under worst case scenarios to thousands of hours of use in best scenarios [2].

The inner spacer is subjected to high electric fields during device operation, making it vulnerable to time-dependent dielectric breakdown (TDDB), a failure mechanism that can lead to premature device degradation. This issue is especially pronounced at the sharp corners of nanosheets, where field crowding exacerbates stress on the dielectric material [4]. Thinner inner spacers can improve device performance but come at the cost of reduced long-term reliability, forcing designers to make tradeoffs between electrical efficiency and robustness. New spacer materials and improved geometric control may help to mitigate these risks.

C. Thermal and Variability Effects

Another significant challenge facing GAAFET technology is self-heating, a thermal issue that can compromise both device performance and reliability. The geometry of GAAFETs—featuring vertically stacked nanosheets and a fully surrounding gate—offers limited thermal conduction pathways for dissipating heat. As a result, localized heat buildup occurs during operation, particularly under high current densities or prolonged switching activity.

This self-heating effect (SHE) accelerates degradation mechanisms such as bias temper-

ature instability (BTI) and hot carrier injection (HCI), both of which reduce transistor lifespan and increase variability [2]. BTI leads to threshold voltage shifts over time due to charge trapping, while HCI results from high-energy carriers damaging the gate dielectric or interface. The impact of SHE is further magnified in stacked structures with multiple nanosheets, where thermal confinement increases as more channels are added.

III. RECENT ADVANCES AND EXPERIMENTAL FINDINGS

Despite the engineering challenges posed by GAAFET development, significant progress has been made across multiple domains, including device reliability, process integration, and nanosheet design optimization. Both industry and academic researchers have contributed to advancing the current state of GAA technology, demonstrating experimental and modeling results that validate the device's viability for sub-5 nm technology nodes.

A. Device Performance and Structure Optimization

A key innovation in modern GAAFET development is the use of wrap-around contacts (WACs), which reduce contact resistance by improving gate-to-source/drain connectivity. These contacts enhance current drive and lower parasitic resistance, supporting the performance needed for high-speed logic applications. WACs are particularly effective for vertically stacked nanosheets, where maintaining uniform contact coverage is otherwise challenging.

Additionally, gate work function engineering and the use of dual work function metals have enabled more precise threshold voltage (V_T) tuning and the development of multi-V_T devices. This provides circuit designers with greater flexibility in optimizing power/performance tradeoffs in complex logic designs. Advancements in extreme ultraviolet (EUV) lithography have also improved patterning accuracy and the channel release process essential to nanosheet fabrication.

B. Compact Modeling for Sub-3nm Circuit Design

To better predict and optimize the behavior of sub-3 nm GAAFETs, compact modeling has become increasingly important. In a study by Mo et al. [7], a nanosheet GAAFET (NS-GAAFET) compact SPICE model was developed and calibrated using 3D device simulations tailored for vertically stacked structures. These models incorporate advanced electrostatic behavior, mobility degradation, parasitic resistance, and gate fringing capacitance to more accurately represent real-world device performance.

Their findings showed that circuit behavior is highly sensitive to nanosheet thickness (T_{NS}), gate length (L_G), and effective channel width (W_{EFF}). While increasing nanosheet count enhances drive current, it also introduces tradeoffs in thermal performance and device variability. The study emphasized that co-optimizing geometry and material parameters—especially source/drain extensions—is essential for balancing performance and manufacturability. Accurate parameter extraction and TCAD-based calibration were also shown to be critical for reliable modeling at the circuit level.

C. Experimental Optimization for Sub-2 nm GAA Nodes

A recent study by Vyas et al. [6] at Applied Materials investigated resistance bottlenecks and their impact on circuit-level performance in first-generation GAAFETs designed for the 2 nm node. Using a calibrated process-device-circuit co-optimization platform, the authors evaluated several physical design strategies targeting ON-resistance (R_{ON}) and drive current (I_{ON}).

Their key findings demonstrated that increasing the nanosheet count from three to four per device led to a 26% improvement in I_{ON}, primarily through reduced channel resistance ($R_{channel}$). Additionally, applying higher source/drain extension doping and introducing local nanosheet trimming significantly lowered extension resistance (R_{SDE}), resulting in a 14% boost in pMOS I_{ON}. WAC integration further reduced contact resistance, providing an additional 4–5

When these optimizations were combined, the total drive current increased by over 50%, while ring oscillator performance improved by 18%, all without reducing gate length or CPP. These results underscore that targeted structural and process optimizations—rather than pure dimensional scaling—can achieve performance enhancements needed for future technology nodes.

IV. Future Directions

While recent advancements have demonstrated promising gains in performance and manufacturability, several key challenges remain as the industry pushes towards sub-2 nm nodes. Future research must focus not only on optimizing the physical structure of the nanosheet devices but also on developing better predictive models, new materials, and innovative integration strategies to support continued logic scaling.

The reliability of the inner space region exacerbates field crowing at the corners of the nanosheet, as mentioned previously. To mitigate breakdown risk, research into new spacer materials, such as hybrid low-k stacks or engineered dielectrics with higher breakdown strength, could improve both electrical isolation and longevity [1]. Additionally, spacer shape engineering, potentially through advanced etch or deposition techniques, may enable more uniform and precise square-profile spacers that reduce field stress.

Another promising direction involves thermal management strategies for vertically stacked nanosheet devices. As demonstrated in recent modeling studies [9], increasing nanosheet count improves performance but worsens self-heating effects. Future device designs may incorporate thermal vias, dielectric isolation layers, or even embedded heat spreaders within the source/drain regions to mitigate these effects. In addition to these hardware innovations, compact thermal-aware models should be developed and integrated into design flows to assess reliability tradeoffs early in the technology development cycle.

Lastly, the emergence of complementary FET (CFET) [8] could be an improvement even

upon GAAFETs. CFETs stack n-type and p-type devices vertically to reduce footprint and increase integration density. These devices are still in early research stages, even still they could benefit from advances made in nanosheet structure technology that GAAFETs will lay the groundwork for. As GAAFET technologies mature, transitioning research efforts toward vertical integration, monolithic 3D stacking, and advanced packaging will be essential to meet future demands for logic density and energy efficiency.

V. SUMMARY AND CONCLUSIONS

GAA transistors represent a pivotal advancement in semiconductor device architecture, enabling CMOS scaling beyond 5 nm node sizes. With better electrostatic control, scalability, and improved drive current, GAAFETs address many limitations faced by FinFETs. Even still, there are challenges that need to be overcome for widespread adoption, including fabrication precision, thermal management, and space reliability. Through recent experimental demonstrations and compact modeling studies, significant strides have been made in mitigating these obstacles via innovations such as wrap-around contacts, nanosheet count optimization, and co-optimized material stacks. The continued evolution of FET architectures is a promising field of stacked nanosheet designs with CFETs that would greatly benefit from GAAFETs being a base of technological support. As the industry continues forward into the Angstrom era, GAAFETs will not only be a crucial technology for solving solutions now but also act a a stepping stone for better high-performance sub-nanoscale nodes

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AUTHOR DECLARATIONS

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